TO THE CLAIMS:

This listing of claims will replace all prior versions, and listings, of claims in the application:

LISTING OF CLAIMS:

1. (currently amended): An apparatus for selectively providing power from a secondary power source, comprising:

a field effect transistor, having a source coupled to the secondary power source, ~~where the secondary power source has a lower potential than a primary power source~~;

a first diode, coupled to a drain of the field effect transistor and to a device to be powered;

a second diode, coupled to the primary power source and the device to be powered; and

an inverter, coupled to the primary power source and to a gate of the field effect transistor, wherein the inverter maintains the field effect transistor in a pinched-off condition and ~~preventing~~prevents a current flow from the secondary power source ~~where~~whenever the primary power source is available.

2. (original): The apparatus of claim 1, wherein the field effect transistor is a depletion mode field effect transistor.

3. (original): The apparatus of claim 2, wherein the depletion mode field effect transistor is an n-channel depletion mode field effect transistor.

4. (original): The apparatus of claim 1, wherein the field effect transistor is an enhancement mode field effect transistor.

5. (original): The apparatus of claim 4, wherein the enhancement mode transistor is a p-channel enhancement mode field effect transistor.

6. (currently amended): An apparatus for selectively providing power from a secondary power source, comprising:

a first diode, coupled between the primary power source and a device to be powered;

a second diode, coupled to the secondary power source~~, where the secondary power source has a lower potential than a primary power source~~;

a field effect transistor, having a source coupled to the second diode and a drain coupled to the first diode~~primary power source~~ and the device to be powered; and

an inverter, coupled to the primary power source and to a gate of the field effect transistor, wherein the inverter maintains the field effect transistor in a pinched-off condition and ~~preventing~~prevents a current flow from the secondary power source ~~when~~whenever the primary power source is available.

7. (original): The apparatus of claim 6, wherein the field effect transistor is a depletion mode field effect transistor.

8. (original): The apparatus of claim 7, wherein the depletion mode field effect transistor is an n-channel depletion mode field effect transistor.

9. (original): The apparatus of claim 6, wherein the field effect transistor is an enhancement mode field effect transistor.

10. (original): The apparatus of claim 9, wherein the enhancement mode transistor is a p-channel enhancement mode field effect transistor.

11. (new): The apparatus of claim 1, further including a reset integrated circuit ("IC") coupled to the inverter.

12. (new): The apparatus of claim 6, further including a reset IC coupled to the inverter.